IN THE CLAIMS:

Claims 1, 17, 24, 26, 51, 67, 74, 75, and 76 have been amended herein. Please cancel claims 25 and 75. Please note that all claims currently pending and under consideration in the referenced application are shown below. Please enter these claims as amended. This listing of claims will replace all prior versions and listings of claims in the application.

Listing of Claims:

1. (currently amended) A method of molding a semiconductor assembly comprising:

providing a transfer mold having an inner surface defining at least one mold cavity;

providing at least one semiconductor substrate having at least one surface with conductive elements thereon and a back surface thereof;

positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate ~~and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate~~;

configuring said portions of said inner surface of said transfer mold to comprise a plurality of recesses formed therein, each recess of said plurality defined by an imperforate boundary wall sized and configured to at least partially substantially conformally receive a portion of corresponding conductive elements protruding from the at least one semiconductor substrate; and

introducing a flowable material onto said at least one surface of said at least one semiconductor substrate in a substantially vertical direction in said at least one mold cavity so that said flowable material flows around said portions of said inner surface of said transfer mold abutting with said conductive elements on said at least one surface of said at least one semiconductor substrate.

2. (previously presented) The method according to claim 1, wherein said providing said transfer mold comprises configuring said transfer mold so that said at least one cavity is substantially vertically oriented with at least one gate at a lower portion of the transfer mold and at least one vent at an upper portion of the transfer mold.

3. (previously presented) The method according to claim 2, wherein said introducing said flowable material comprises:
substantially filling said at least one cavity in said substantially vertical direction.

4. (previously presented) The method according to claim 3, wherein said substantially filling said at least one cavity comprises:
introducing said flowable material through said at least one gate until a single flow front of said flowable material contacts said at least one vent at said upper portion of said at least one cavity.

5. (previously presented) The method according to claim 2, wherein said positioning said at least one semiconductor substrate further comprises:
positioning said at least one semiconductor substrate substantially vertically.

6. (previously presented) The method according to claim 4, wherein said introducing said flowable material comprises:
filling said at least one cavity until a single flow front of said flowable material contacts said at least one vent.

7. (previously presented) The method according to claim 6, wherein said filling said at least one cavity with said flowable material comprises:
at least partially encapsulating said at least one semiconductor substrate.

8. (original) The method according to claim 1, wherein said introducing said flowable material in said substantially vertical direction comprises:
inducing a substantially uniform flow front.

9. (previously presented) The method according to claim 1, wherein said introducing said flowable material comprises introducing said flowable material onto a substantially vertically oriented surface of said at least one semiconductor substrate.

10. (previously presented) The method according to claim 1, wherein said introducing said flowable material onto said at least one surface of said at least one semiconductor substrate in said substantially vertical direction comprises:
substantially preventing voids in said flowable material.

11. (previously presented) The method according to claim 1, wherein said providing said at least one semiconductor substrate comprises:
providing an assembly including said at least one semiconductor substrate.

Claim 12. (canceled)

13. (previously presented) The method according to claim 11, wherein said providing said assembly comprises:
providing said assembly with said at least one semiconductor substrate comprising at least one semiconductor die having said conductive elements in the form of bond pads thereon, said at least one semiconductor die including conductive structures protruding from said bond pads.

Claims 14-15. (canceled)

16. (previously presented) The method according to claim 1, wherein said providing said at least one semiconductor substrate comprises:
providing at least one individual semiconductor die.

17. (currently amended) The method according to claim 16, wherein said providing said at least one individual semiconductor die comprises:
providing said at least one individual semiconductor die with conductive structures protruding therefrom to be received by and abut with said portions of said at least one cavity.

18. (previously presented) The method according to claim 1, wherein said providing said at least one semiconductor substrate comprises:
providing a large-scale semiconductor substrate.

19. (previously presented) The method according to claim 18, wherein said providing said large-scale semiconductor substrate comprises:
providing a plurality of semiconductor dice interconnected to each other, each of said plurality comprising said conductive elements in the form of bond pads and conductive structures protruding from said bond pads.

20. (previously presented) The method according to claim 18, wherein said providing said large-scale semiconductor substrate comprises:
providing at least a portion of a wafer.

21. (previously presented) The method according to claim 1, wherein said introducing said flowable material includes capillary action acting on said flowable material.

22. (previously presented) The method according to claim 1, wherein said introducing said flowable material includes positive pressure acting on said flowable material.

23. (previously presented) The method according to claim 1, wherein said introducing said flowable material includes negative pressure acting on said flowable material.

24. (currently amended) The method according to claim 6, wherein said filling said at least one cavity with said flowable material comprises substantially completely encapsulating said at least one semiconductor substrate.

~~The method according to claim 1, wherein said providing said transfer mold comprises configuring said portions of said inner surface of said transfer mold to comprise protrusions to abut with said conductive element on said at least one surface of said at least one semiconductor substrate so that said flowable material partially covers said at least one surface of said at least one semiconductor substrate.~~

Claim 25. (cancelled)

26 (currently amended) The method according to claim 1, wherein providing at least one semiconductor substrate having at least one surface with conductive elements thereon comprises providing at least one semiconductor substrate having at least one surface with conductive columns or pillars. ~~A method of molding a semiconductor assembly comprising:~~

~~providing a transfer mold having an inner surface defining at least one mold cavity;~~

~~providing an assembly including at least one semiconductor device attached face down to a carrier substrate with conductive structures providing an assembly gap therebetween;~~

~~positioning said assembly in said at least one mold cavity of said transfer mold so that said carrier substrate abuts with a first inner surface of said transfer mold to provide an outer gap between a back surface of said at least one semiconductor device and an opposing second inner surface of said transfer mold; and~~

~~introducing a flowable material onto at least one surface of said assembly to flow through said assembly gap and said outer gap in an upward, substantially vertical direction in said at least~~

~~one mold cavity.~~

Claims 27-50. (canceled)

51. (currently amended) A method for encapsulating a substrate that substantially prevents voids in an encapsulant, the method comprising:

providing a transfer mold having an inner surface defining at least one mold cavity;

providing at least one semiconductor substrate having at least one surface with conductive elements thereon and a back surface thereof;

positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate~~ and another portion of said inner surface abuts with said back surface of said at least one semiconductor substrate~~;

configuring said portions of said inner surface of said transfer mold to comprise a plurality of recesses formed therein, each of said recesses having an imperforate boundary wall sized and configured to at least partially substantially conformally receive a portion of a corresponding conductive element protruding from the at least one semiconductor substrate; and

introducing a flowable material onto said at least one surface of said at least one semiconductor substrate in an upward, non-horizontal direction in said at least one mold cavity so that said flowable material flows around said portions of said inner surface of said transfer mold abutting with said conductive elements on said at least one surface of said at least one substrate.

52. (previously presented) The method according to claim 51, wherein said providing said transfer mold comprises configuring said transfer mold so that said at least one cavity is non-horizontally oriented with at least one gate at a lower portion of the transfer mold and at least one vent at an upper portion of the transfer mold.

53. (previously presented) The method according to claim 52, wherein said introducing said flowable material comprises:
substantially filling said at least one cavity in a non-horizontal direction.

54. (previously presented) The method according to claim 53, wherein said substantially filling said at least one cavity comprises:
introducing said flowable material through said at least one gate until a single flow front of said flowable material contacts said at least one vent at said upper portion of said at least one cavity.

55. (previously presented) The method according to claim 52, wherein said positioning said at least one semiconductor substrate further comprises:
positioning said at least one semiconductor substrate substantially vertically.

56. (previously presented) The method according to claim 55, wherein said introducing said flowable material comprises:
filling said at least one cavity until said single flow front of said flowable material contacts said at least one vent.

57. (previously presented) The method according to claim 56, wherein said filling said at least one cavity with said flowable material comprises:
at least partially encapsulating said at least one semiconductor substrate.

58. (previously presented) The method according to claim 51, wherein said introducing said flowable material in said upward, non-horizontal direction comprises:
inducing a substantially uniform flow front.

59. (previously presented) The method according to claim 51, wherein said introducing said flowable material comprises permitting said flowable material to flow onto a substantially vertically oriented surface of said at least one semiconductor substrate.

60. (previously presented) The method according to claim 51, wherein said introducing said flowable material onto said at least one surface of said at least one substrate in said upward, non-horizontal direction comprises:
substantially preventing voids in said flowable material.

61. (previously presented) The method according to claim 51, wherein said providing said at least one semiconductor substrate comprises:
providing an assembly including said at least one semiconductor substrate.

Claim 62. (canceled)

63. (previously presented) The method according to claim 61, wherein said providing said assembly comprises:
providing said assembly with said at least one semiconductor substrate including at least one semiconductor die having said conductive elements in the form of bond pads thereon, said at least one semiconductor die including conductive structures protruding from said bond pads.

Claims 64-65. (canceled)

66. (previously presented) The method according to claim 51, wherein said providing said at least one semiconductor substrate comprises:
providing at least one individual semiconductor die.

67. (currently amended) The method according to claim 66, wherein said providing said at least one individual semiconductor die comprises:
providing said at least one individual semiconductor die with conductive structures protruding therefrom to be received by and abut with said portions of said at least one cavity.

68. (previously presented) The method according to claim 51, wherein said providing said at least one semiconductor substrate comprises:
providing a large-scale semiconductor substrate.

69. (previously presented) The method according to claim 68, wherein said providing said large-scale semiconductor substrate comprises:
providing a plurality of semiconductor dice interconnected to each other, each of said plurality comprising at least one of bond pads and conductive structures protruding from said bond pads.

70. (original) The method according to claim 68, wherein said providing said large-scale substrate comprises:
providing at least a portion of a wafer.

71. (previously presented) The method according to claim 51, wherein said introducing said flowable material includes capillary action acting on said flowable material.

72. (previously presented) The method according to claim 51, wherein said introducing said flowable material includes positive pressure on said flowable material.

73. (previously presented) The method according to claim 51, wherein said introducing said flowable material includes negative pressure on said flowable material.

74. (currently amended) The method according to claim 56, wherein said filling said at least one cavity with said flowable material comprises at least partially encapsulating said at least one semiconductor substrate.

~~The method according to claim 51, said providing said transfer mold comprises configuring said portions of said inner surface of said transfer mold to comprise protrusions to abut with said conductive element on said at least one surface of said at least one semiconductor substrate so that said flowable material partially covers said at least one surface of said at least one semiconductor substrate.~~

75. (cancelled)

76. (currently amended) The method according to claim 51, wherein providing at least one semiconductor substrate having at least one surface with conductive elements thereon comprises providing at least one semiconductor substrate having at least one surface with conductive columns or pillars. ~~A method for transfer molding a semiconductor assembly comprising:~~

~~providing at least one transfer mold having an inner surface defining at least one cavity, said at least one transfer mold including at least one gate at a lower portion thereof and at least one vent at an upper portion thereof;~~

~~providing an assembly including at least one semiconductor device attached face down to a carrier substrate with conductive structures providing an assembly gap therebetween;~~

~~positioning said assembly in said at least one mold cavity of said transfer mold so that said carrier substrate abuts with a first inner surface of said transfer mold to provide an outer gap between a back surface of said at least one semiconductor device and an opposing second inner~~

~~surface of said transfer mold; and~~

~~introducing a resin material into said at least one cavity through said at least one gate so that said resin material moves upwardly over said assembly and through said assembly gap and said outer gap in a non-horizontal direction.~~

Claims 77-98. (canceled)

REMARKS

The Final Office Action mailed July 29, 2003, has been received and reviewed. Claims 1 through 11, 13, 16 through 25, 51 through 61, 63, and 66 through 75 are currently pending in the application. Claims 1 through 11, 13, 16 through 25, 51 through 61, 63, and 66 through 75 stand rejected. However, the body of the July 29, 2003 Office Action does not state a basis for rejection of claims 22, 23, 72, and 73. Applicant kindly requests a clarification as to the status of claims 22, 23, 72, and 73. Applicant proposes to amend claims 1, 17, 24, 25, 26, 51, 67, 74, 75, and 76 and respectfully requests reconsideration of the application as proposed to be amended herein.

Information Disclosure Statement(s)

Applicant notes the filing of a Supplemental Information Disclosure Statement and Form PTO/SB/08 herein on July 30, 2003, one day after the mailing date of the outstanding final office action. Because these documents were previously submitted without the $180.00 fee required for submissions after the mailing date of a final office action, Applicant resubmitted the Supplemental Information Disclosure Statement and Form PTO/SB/08 on August 12, 2003, enclosing a check in the amount of $180.00 to cover the required fee. Applicant respectfully requests that the information cited on the PTO/SB/08 be made of record herein, and that a copy of the PTO/SB/08, as initialed by Examiner, be returned to Applicant's counsel.

35 U.S.C. § 102(b) Anticipation Rejections

Anticipation Rejection Based on Japanese Patent No. JP53163977 to Takemoto

Claims 1 and 51 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent No. JP53163977 to Takemoto ("Takemoto"). Applicant respectfully traverses this rejection, as hereinafter set forth.

A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention

must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Independent claim 1, as presently amended, includes positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and configuring said portions of said inner surface of said transfer mold to comprise recesses formed therein, each recess of said plurality defined by an imperforate boundary wall sized and configured to at least partially substantially conformally receive a portion of corresponding conductive elements protruding from the at least one semiconductor substrate.

Independent claim 51, as presently amended, includes positioning said at least one semiconductor substrate in said at least one mold cavity of said transfer mold so that portions of said inner surface of said transfer mold abut with said conductive elements of said at least one surface of said at least one semiconductor substrate and configuring said portions of said inner surface of said transfer mold to comprise recesses formed therein, each of said recesses having an imperforate boundary wall sized and configured to at least partially substantially conformally receive a portion of a corresponding conductive element protruding from the at least one semiconductor substrate.

Although the Office Action asserts that "inherently the semiconductor surface abutting the cavity *may have* microstructure protruding from the surface of such a dimension that they are not shown in detail from the macroscopic perspective," Applicant respectfully submits that this assertion does not establish inherency.

Rather, M.P.E.P. § 2112 explains that the fact that a certain result or characteristic may occur or be present in the prior art is not sufficient to establish the inherency of that result or characteristic. *See* M.P.E.P. § 2112, citing *In re Rijckaert*, 9 F.3d 1531, 1534, 28 USPQ2d 1955, 1957 (Fed. Cir. 1993); In re Oelrich, 666 F.2d 578, 581-82, 212 USPQ 323, 326 (CCPA 1981).

Therefore, Applicant respectfully submits that even assuming that the semiconductor surface abutting the cavity *may have* microstructure protruding from the surface of such a dimension that they are not shown in detail from the macroscopic perspective, as stated in the

Office Action, inherency of such conductive structures by way of the Takemoto reference has not been established.

However, further assuming, *arguendo*, that such protruding elements are inherent, Takemoto fails to disclose that each recess is defined by an imperforate boundary wall sized and configured to at least partially substantially conformally receive a portion of corresponding conductive elements protruding from the at least one semiconductor substrate, whatsoever.

Additionally, independent claim 1 includes introducing a flowable material *onto said at least one surface* of said at least one semiconductor substrate in a substantially vertical direction. Emphasis added.

Further, independent claim 51includes introducing a flowable material *onto said at least one surface* of said at least one semiconductor substrate in an upward, non-horizontal direction. Emphasis added.

In the Office Action, Page 5, it is asserted that Takemoto discloses the limitation because the input port is below the surface of the semiconductor. Further, the Office Action states that the flowing material must approach the surface from a vertical orientation. However, claims 1 and 51 include introducing a flowable material *onto the surface* in a substantially vertical direction and in an upward, non-horizontal direction, respectively. Thus, Applicant respectfully submits that claims 1 and 51 describe the introducing of flowable material in relation to the surface, whereas the Office Action appears to rewrite the claim limitation to apply to the flowable material introduction in relation to the mold cavity.

Further, Applicant respectfully submits that Takemoto does not even disclose that the mold cavity would fill with encapsulant in a vertical manner. Rather, Applicant respectfully submits that it appears that the Office Action *assumes* that a vent is located at the upper surface of the mold. However, FIG. 4 of Takemoto does not appear to disclose the position of any vent. Therefore, the mold may very well fill from the input port 12 *which is positioned laterally to one side (right)* and fill the mold therefrom ***laterally, from right to left.*** Applicant respectfully submits that Takemoto does not teach the identical invention in as complete detail as contained in the claim.

Even assuming, *arguendo*, that the mold cavity as disclosed by Takemoto fills vertically, Applicant respectfully submits that encapsulant introduced within the mold as disclosed by Takemoto, of necessity, moves, *in relation to the surface of the semiconductor,* in a horizontal direction with all of the attendant disadvantages pointed out in Applicant's specification. Therefore, Applicant respectfully submits that it appears from FIG. 4 that flowable material would be introduced to the upper or lower horizontal surfaces of the semiconductor (if flowable material flows thereon whatsoever) in a horizontal direction.

Similarly, as to independent claim 51, Applicant respectfully submits that Takemoto fails to disclose each and every element of the claim limitation of introducing a flowable material onto said at least one surface of said at least one semiconductor substrate in an upward, non-horizontal direction.

Accordingly, Applicant respectfully submits that Takemoto fails to disclose each and every element of independent claims 1 and 51 in as complete detail as is contained in the claims.

Applicant respectfully requests reconsideration and allowance of independent claims 1 and 51.

35 U.S.C. § 103(a) Obviousness Rejections

Obviousness Rejection Based on Japanese Patent No. JP53163977 to Takemoto and Further in View of Japanese Patent No. JP06151492 to Sony Corporation

Claims 2 through 11, 16 through 21, 24, 52 through 61, 63, 66 through 71, and 74 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takemoto (Japanese Patent No. JP53163977), as applied to claims 1 and 51 above, and further in view of Sony Corporation (Japanese Patent No. JP06151492). Applicant respectfully traverses this rejection, as hereinafter set forth.

M.P.E.P. 706.02(j) sets forth the standard for a Section 103(a) rejection:

> To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or combine reference teachings. Second, there must be a reasonable expectation of success. Finally, **the prior art reference (or references when combined) must teach or suggest all the claim limitations.**

> The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991). (Emphasis added).

The 35 U.S.C. § 103(a) obviousness rejections are improper because claims 2 through 11, 16 through 21, 24, 52 through 61, 63, 66 through 71, and 74 are each allowable as respectively depending from an allowable independent claim.

Applicant respectfully requests reconsideration and allowance of claims 2 through 11, 16 through 21, 24, 52 through 61, 63, 66 through 71, and 74.

Obviousness Rejection Based on Japanese Patent No. JP53163977 to Takemoto in View of Japanese Patent No. JP06151492 to Sony Corporation, and Further in View of U.S. Patent No. 6,081,997 to Chia et al.

Claims 13, 25, 63, and 75 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Takemoto (Japanese Patent No. JP53163977) in view of Japanese Patent No. JP06151492 to Sony Corporation ("Sony"), as applied to claims 1 through 11, 16 through 21, 24, 51 through 61, 66 through 71, and 74 above, and further in view of U.S. Patent No. 6,081,997 Chia et al. ("Chia"). Applicant respectfully traverses this rejection, as hereinafter set forth.

Claims 25 and 75 have been cancelled.

Claim 13 depends from independent claim 1, which is allowable. Accordingly, Applicant respectfully requests reconsideration and allowance of dependent claim 13.

Takemoto is silent as to teaching or suggesting recesses and, therefore, is also silent as to sizing or configuring any such recesses. Likewise, Sony and/or Chia are each silent as to teaching or suggesting recesses and, thus are each also silent about sizing or configuring any such recesses.

The Office Action states that "wherein cavity at least partially receives protruding structures (inherently the semiconductor surface abutting the cavity may have microstructure protruding from the surface of such a dimension that they are not shown in detail from the macroscopic perspective) of said at least one substrate." Page 4, last two lines, Page 5, lines 1-3.

To the extent understood, it appears the Office Action relies on inherent protruding structures and inherent receiving recesses which *may* exist, none of which are illustrated or described in the references.

Applicant respectfully submits that inherency as to recesses has not been established as discussed hereinabove in relation to the asserted inherency of protrusions.

Further, Applicant respectfully submits that none of Takemoto, Sony, or Chia teach or suggest configuring the recesses.

Dependent claim 63 is allowable as depending from independent claim 51, which is allowable. Applicant respectfully requests reconsideration and allowance of dependent claim 63.

ENTRY OF AMENDMENTS

The proposed amendments to claims 1, 17, 24, 26, 51, 67, 74, and 76 above should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application. Applicant respectfully submits that FIG. 7 and paragraph [0031] support the amendments to claims 24 through 26 and 74 through 76. Further, the amendments do not raise new issues or require a further search. Finally, if the Examiner determines that the amendments do not place the application in condition for allowance, entry is respectfully requested upon filing of a Notice of Appeal herein.

CONCLUSION

Claims 1-76 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicant's undersigned representative.

Respectfully submitted,

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Date: September 10, 2003
JAW/ps:ljb
Document in ProLaw